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TRANSMITTAL FORM

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Total Number of Pages in This Submission	

Application Number	08/841,644
Filing Date	April 30, 1997
First Named Inventor	Shunpei YAMAZAKI et al.
Group Art Unit	2813
Examiner Name	L. Schillinger
Attorney Docket Number	0756-1603

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
- ☐ Drawing(s)
- ☐ Declaration and Power of Attorney
- ☐ Licensing-related Papers
- ☐ Petition
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
- ☐ After Allowance Communication to Group
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- ☐ Proprietary Information
- ☐ Status Letter
- ☐ Other Enclosures
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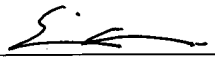
Remarks

☒ The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-2280 for the above identified docket number.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	Eric J. Robinson, Reg. No. 38,285 Robinson Intellectual Property Law Office, P.C. PMB 955 21010 Southbank Street Potomac Falls, VA 20165
Signature	
Date	June 21, 2006

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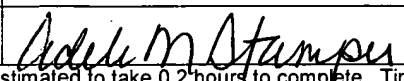
Signature		Date	June 21, 2006

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Attorney Docket No. 0756-1603

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Group Art Unit: 2813
Shunpei YAMAZAKI et al.	)	Examiner: Laura M. Schillinger
Serial No. 08/841,644	)	CERTIFICATE OF MAILING
Filed: April 30, 1997	)	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on June 21, 2006
For: SEMICONDUCTOR DEVICE AND METHOD FOR FORMING THE SAME	)	Adele M. Stamper

RESPONSE

Honorable Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The Official Action mailed March 21, 2006, has been received and its contents carefully noted. This response is filed within three months of the mailing date of the Official Action and therefore is believed to be timely without extension of time. Accordingly, the Applicant respectfully submits that this response is being timely filed.

The Applicant notes with appreciation the consideration of the Information Disclosure Statements filed on September 22, 1997; December 9, 1998; August 18, 1999; October 14, 1999; April 13, 2000; July 25, 2000; November 8, 2000; June 25, 2001; May 15, 2002; May 22, 2002; June 27, 2003; and September 28, 2004.

Claims 23-32 are pending in the present application, of which claims 23 is independent. For the reasons set forth in detail below, all claims are believed to be in condition for allowance. Favorable reconsideration is requested.

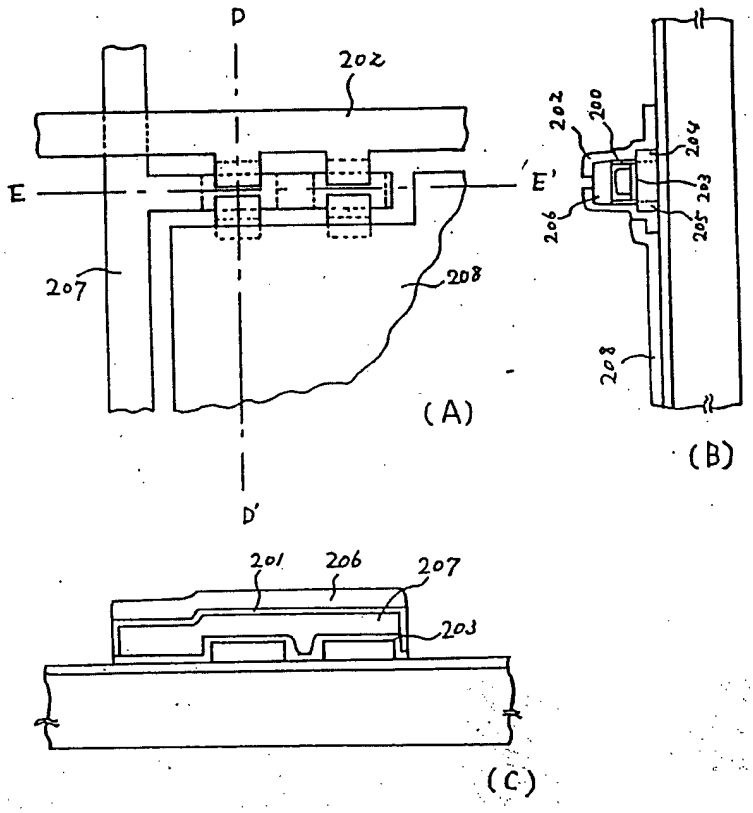
The Official Action rejects claims 23-32 under 35 U.S.C. § 112, first paragraph, asserting that some of the features of claim 23 are not supported in the present specification. The Official Action asserts that the chart fails to show support for the recitation "simultaneously forming an overlying gate insulator on a top and sidewalls of

said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line." Specifically, the Official Action asserts that "Applicant's specification fails to teach anodic oxidation of the gate line at all, let alone doing so simultaneously with the gate electrode" (page 3, Paper No. 030506). The Applicant respectfully disagrees and traverses the above-referenced assertions in the Official Action.

The present specification supports the recitation of simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line. As noted in detail at the bottom of page 1 and at the top of page 2 of the chart originally submitted with the *Preliminary Amendment* filed April 30, 1997 (resubmitted December 1, 2005), Figures 1, 3G and 4, and the disclosure at pages 6 and 7 show and describe an anodic oxide film covering both a gate electrode and a gate wiring.

Furthermore, Figure 14 (reproduced below), for example, supports the recitation of simultaneously forming an overlying gate insulator on a top and sidewalls of said gate electrode and said gate line by anodic oxidation of said gate electrode and said gate line to reduce the dimensions of said gate electrode and said gate line.

Fig. 14



For example, the present specification describes a gate wiring (or gate line) (e.g. left side of 207 as shown in Figures 14A and 14C), which is in electrical contact with a gate electrode (e.g. right side of 207 as shown in Figures 14A and 14C). Both the gate wiring and the gate electrode may be formed between gate insulating film (e.g. 203) and anodically oxided film (e.g. 201). That is, both the gate electrode and the gate wiring are formed on the same layer (gate insulating film 203). Hence, neither the gate wiring nor the gate electrode is blocked by another layer. As such, a simultaneous anodic oxidation occurs on the gate wiring and the gate electrode, as shown, for example, in Figure 14 (see also, e.g., Example 3, pages 35-36). Therefore, the present specification teaches simultaneously forming an overlying gate insulator on a top and

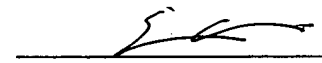
sidewalls of said gate electrode and said gate line 207 by anodic oxidation of said gate electrode and said gate line.

The Applicant respectfully submits that claims 23-32, when read in light of the specification, are adequately described and supported in the specification. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 112 are in order and respectfully requested.

For the reasons noted in detail in the above-referenced *Preliminary Amendment*, the Applicant respectfully requests that they be designated senior party in a declaration of interference with respect to U.S. Patent No. 5,561,075 to Nakazawa.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



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